Guidelines for design research

I. Your research should include five sections:

1) Introduction
2) Design
3) results
4) Assembly program
5) references

II. formatting:

1) paper size A4
2) font type times new roman
3) font size 14
4) spacing 1.5
5) alignment justify
6) page number on every page

note: there will be template on your course site which contains all these requirements.

Deign a processor that is register to register architecture, write an assembly program for that processor.

1) **Introduction**

In this section, you will write a brief description of your processor (components, microoperations) and specify the size of each component.

- Number of register you can use at minimum 3 registers. Choose the number that facilitate your work
- The main microoperations should be included in your processor

  ADD R, R, R

  MUL R, R, R
- You are free to choose any size of memory.
- You are free to specify the ALU operations.

2) **Design**

You have two options; by hardware or VHDL.

- If you choose to design by Hardware.

  -Write your RTL
- If you choose to design by VHDL.

  -Write your code associated with comments.

3) **Implementation/Results**

- *If you choose to design by Hardware in sec. 3:*

  Draw your hardware blocks i.e. indicating the control gates connected to each blocks and the connections between different blocks
- *If you choose to design by VHDL in sec. 3:*

  Screen shoots of your simulation results.

4) **Assembly program**

Write an assembly program implemented by your processor for any simple c++ program.

5) **References**

If your reference is **book:** **The author(s), The title**, book.

If your reference is **lecture notes:** The author(s), year, The title, Lectures note, University.

If your reference is **URL:** URL, Access time

Deign a processor that is accumulator based architecture, write an assembly program for that processor.

1) **Introduction**

In this section, you will write a brief description of your processor (components, microoperations) and specify the size of each component.

- the main microoperations should be included in your processor

ADD	MEM	(MEM← AC + MEM)
SUB	MEM	(AC ← MEM –AC)
MUL	MEM	(AC ← AC * MEM)
FAC	MEM	(AC ← MEM!)

- You are free to choose any size of memory.
- You are free to specify the ALU operations.

2) **Design**

You have two options; by hardware or VHDL.

- If you choose to design by Hardware.

  -Write your RTL

- If you choose to design by VHDL.

  -Write your code associated with comments.

3) **Implementation/Results**

- *If you choose to design by Hardware in sec. 3:*

  Draw your hardware blocks i.e. indicating the control gates connected to each blocks and the connections between different blocks

- *If you choose to design by VHDL in sec. 3:*

  Screen shoots of your simulation results.

4) **Assembly program**

Write an assembly program implemented by your processor for any simple c++ program.

5) **References**

If your reference is **book:** **The author(s), The title**, book.

If your reference is **lecture notes:** The author(s), year, The title, Lectures note, University.

If your reference is **URL:** URL, Access time

Deign a processor that is register to memory architecture, write an assembly program for that processor.

1) **Introduction**

In this section, you will write a brief description of your processor (components, microoperations) and specify the size of each component.

- Number of register you can use at minimum 3 registers. Choose the number that facilitate your work
- The main microoperations should be included in your processor

  ADD R, R,MEM

  SUB MEM, R, MEM
- You are free to choose any size of memory.
- You are free to specify the ALU operations.

2) **Design**

You have two options; by hardware or VHDL.

- If you choose to design by Hardware.

  -Write your RTL
- If you choose to design by VHDL.

  -Write your code associated with comments.

3) **Implementation/Results**

- *If you choose to design by Hardware in sec. 3:*

  Draw your hardware blocks i.e. indicating the control gates connected to each blocks and the connections between different blocks
- *If you choose to design by VHDL in sec. 3:*

  Screen shoots of your simulation results.

4) **Assembly program**

Write an assembly program implemented by your processor for any simple c++ program.

5) **References**

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If your reference is **URL:** URL, Access time

Guidelines for the comparative study research

a) Your research should include six sections:

1) Introduction
2) Computer architecture classification survey
3) Assembly languages survey
4) Instruction cycles survey
5) summary
6) references

b) Formatting:

1) paper size A4
2) font type times new roman
3) font size 14
4) spacing 1.5
5) alignment justify
6) page number on every page

note: there will be template on your course site which contains all these requirements.

Comparative study of computer architecture classification, assembly languages for different architecture, instruction cycles for different processors.

1) **Introduction**

   In this section, you give a brief introduction about what you will discuss in the following sections.

2) **Computer architecture classification survey**

   There are different classifications for computer architecture as mentioned in your lecture. Try to compare between these architectures and support your comparison by giving example for each architecture.

3) **Assembly languages survey**

   Compare between different assembly languages. Try to compare at least one assembly language for each architecture type (register to register, register to memory, accumulator based)

4) **Instruction cycles survey**

   Instruction cycle can consist of different number of phases (three, two, four…). There are different elements that you can use in comparison; no of phases, brief explanation, advantages, disadvantages ….. etc.

5) **Summary**

   Summarize your work.

6) **References**

   If your reference is **book:** **The author(s), The title**, book.

   If your reference is **lecture notes:** The author(s), year, The title, Lectures note, University.

   If your reference is **URL:** URL, Access time