1. a. **Design** a common bus system between 4 registers (R1, R2, R3 and R4) each of 4-bits using tri-state buffers and decoders.

**Answer:**

b. Starting from an initial value of R = 11001001, **determine** the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.

Answer:

| Micro-operation | R |
|---|---|
| Initially | 11001001 |
| R ← shl R | 10010010 |
| R ← cir R | 01001001 |
| R ← shr R | 00100100 |
| R ← cil R | 01001000 |

c. A digital computer has a common BUS system for 4 registers of 16-bit each; this bus system uses MUXs and a decoder to allow data transfer between any two registers at a time. For this system do the following:

i. How many multiplexers are there in the bus?

16 MUXs

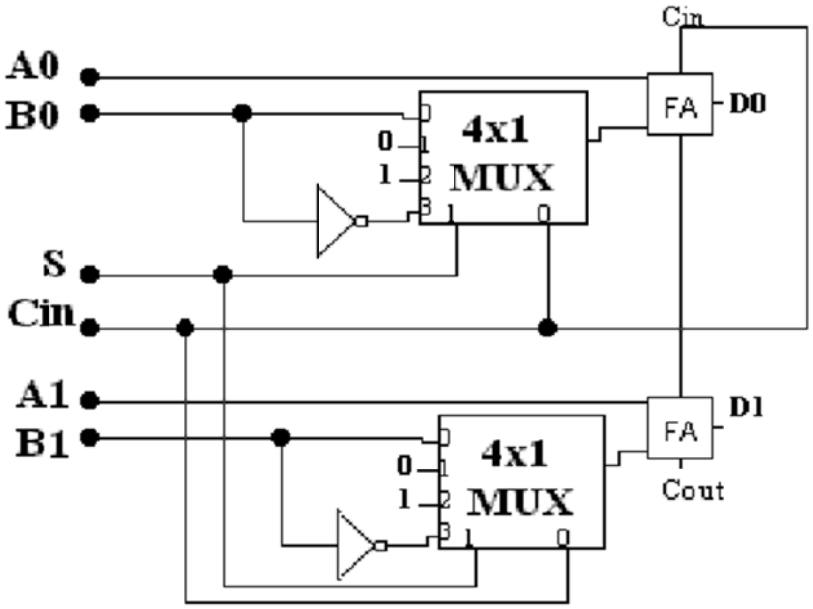
ii. What is the size of each multiplexer?

4X1 MUX's

2. **Design** an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following 4 arithmetic operations in conjunction with the input carry $C_{in}$. **Draw** the logic diagram for the first two stages.

| S | $C_{in}=0$ | $C_{in}=1$ |
|---|---|---|
| 0 | D = A+B (add) | D=A+1 (increment) |
| 1 | D = A-1 (decrement) | D=A+B'+1 (subtract) |

**Answer:**



3. The following control inputs are active in the bus system shown in Fig.(1). For each case, **specify** the register transfer that will be executed during the next clock transition

| | S2 | S1 | S0 | LD of register | Memory | Adder |
|---|---|---|---|---|---|---|
| a. | 1 | 1 | 1 | IR | Read | -- |
| b. | 1 | 1 | 0 | PC | -- | -- |
| c. | 1 | 0 | 0 | DR | Write | -- |
| d. | 0 | 0 | 0 | AC | -- | Add |

**Answer:**

| Question | S2 | S1 | S0 | LD of register | Memory | Adder | Solution |
|---|---|---|---|---|---|---|---|
| A | 1 | 1 | 1 | IR | Read | --- | IR <-- M[AR] |
| B | 1 | 1 | 0 | PC | --- | --- | PC <-- TR |
| C | 1 | 0 | 0 | DR | Write | --- | DR <- AC,M[AR] <-- AC |
| d | 0 | 0 | 0 | AC | --- | Add | AC <- AC + DR |

4. Consider the basic computer registers connected to a common bus system shown in Fig.(1). For each indicated micro-instruction, **complete** the following table:

| Microinstruction | Bus select | | | Source *Register* | Destination Register | | | | Memory | |
|---|---|---|---|---|---|---|---|---|---|---|
| | S2 | S1 | S0 | | *Name* | LD | INR | CLR | Read | Write |
| AR ← PC | **0** | **1** | **0** | **PC** | **AR** | **1** | **0** | **0** | **0** | **0** |
| PC ← PC+1 | **0** | **1** | **0** | **PC** | **PC** | **0** | **1** | **0** | **0** | **0** |
| IR ← M[AR] | **1** | **1** | **1** | **M** | **IR** | **1** | **0** | **0** | **1** | **0** |
| AR ← IR | **1** | **0** | **1** | **IR** | **AR** | **1** | **0** | **0** | **0** | **0** |
| DR ← M[AR] | **0** | **1** | **1** | **M** | **DR** | **1** | **0** | **0** | **1** | **0** |
| TR ← 0 | **0** | **0** | **0** | **TR** | **TR** | **0** | **0** | **1** | **0** | **0** |

5. The register transfer statements for a register R and the memory in a computer are as follows (the X's are control functions)

| | | |
|---|---|---|
| $X_3'X_1$: | R ← M[AR] | Read Memory word into R |
| $X_1'X_2$: | R ← AC | Transfer AC to R |
| $X_1'X_3$: | M[AR] ← R | Write R to Memory |

The memory has data inputs, data outputs, address inputs, and control inputs to read and write. **Draw the hardware implementation of R and the memory in block diagram form**.

**Answer:**